IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph beginning at page 5, line 3 is amended as follows:

The data retention problem and read disturb problem have prevented applications of GSCD in the past. These problems are capable of being designed out of the conventional SSCD by applying an oxide insulator at the floating gate - substrate interface with a high barrier height of 3.2 ev, by applying a thicker oxide-nitride-oxide (ONO) layer on the top and side of the floating gate such that the equivalent oxide thickness ($t_{ox.eq.}$) between the control gate and the floating gate is greater than 70nm, and by selecting the cell geometry (by enlarging the cell size) to achieve a larger coupling ratio ~~ration~~ (K>0.5). For GSCD devices, such approaches with K<0.5 require higher write/erase voltages and result in slower write/erase speeds. Any attempt to improve speed by reducing the insulator thickness between the control gate and the floating gate or lowering the barrier height of the insulator between the control gate and the floating gate enhances the data retention and read disturb problems such that a frequent refresh is needed to prevent data loss.

The paragraph beginning at page 12, line 10 is amended as follows:

Figure 2 is a band diagram illustrating one embodiment of an asymmetric band-gap gate stack incorporated in the device of Figure 1. The band diagram is useful for illustrating the charge transport and charge storage during device operation. The band diagram includes representations for the silicon substrate 202, the aluminum control gate 214, and the asymmetric gate stack 212 between the substrate and the control gate. One embodiment of the asymmetric gate stack 212 includes a first insulator region 216 that includes ~ 2 nm of SiO_2 222[[,]] and ~ 3 - 5 nm $t_{ox.eq.}$ of Ta_2O_5 224, a silicon floating gate 218, and a second insulator region 220 that includes ~ 3 - 5 nm $t_{ox.eq.}$ of ZrO_2 226.

The paragraph beginning at page 15, line 10 is amended as follows:

Figure 4 illustrates charge transport for a Write Process defined as a transition from a conducting low threshold (0) to a nonconducting high threshold (1), using the band diagram of

Figure 2. During the write process, a +12 V programming voltage is applied to the substrate via the drain diffusion as shown in Figure 6, while the control gate is grounded to 0 V. It is noted that the programming voltage is brought into the specific cell via its drain (n+) diffusion while the substrate is made to float. During such process, the channel of the specific cell gets capacitively coupled and rises to the same potential as the drain. In one embodiment, if a block of cells is to be written simultaneously, the relevant substrate block and drain nodes are held together during such writing process. Prior to the writing onset, the specific cell holds a built-in positive potential at the floating gate due to the trapped holes (being in the erased conducting state). During writing, the substrate potential rises to +12 V and with coupling coefficient of the cell designed to be $k<0.5$, more than half of the 12 Volts is imposed between the [[te]] floating gate and the control gate. This potential is further enhanced by the built-in potential of the holes in the floating gate. As a result, the field (EMF) between the floating gate and the control gate attains significantly higher value as compared to that between the substrate and the floating gate at the onset of the writing process. This high field induces hole emission and transport 436 from the floating gate to the control gate. Simultaneously, this high field also induces complementary electron injection and transport 438 from the control gate to the floating gate as shown in Figure 4. Mechanism 436 involves the positive charge removal from the floating gate while mechanism 438 involves positive charge neutralization and or negative charge storage into the floating gate. Both of these involves positive charge neutralization and or negative charge storage into the floating gate. Both of these mechanisms are expected to dominate during the writing process resulting in net negative charge storage in the floating gate and transition of the cell to the non-conducting high threshold state. Some loss of electrons from the silicon floating gate to the silicon substrate defined as mechanism 440 is feasible at the initial transient period when the field associated with the floating gate and the substrate is maximum. But this mechanism is relatively weak due to the low field ($k<0.5$) between the floating gate and the substrate. This is represented by an arrow of intermediate thickness. The remaining mechanism 442, as shown in Figure 4, is insignificant due to the high hole energy barrier of 4.7 ev and the low field across SiO_2-Ta_2O_5 between the silicon substrate and the silicon floating gate. This is represented by a thinner arrow. Therefore, primary charge transport between the silicon floating gate and the aluminum control gate is also maintained by this invention during the write process.

The paragraph beginning at page 18, line 26 is amended as follows:

Figure 8 illustrates one embodiment of a floating plate embodiment of the nonvolatile device of the present invention. The device is similar to that shown in Figure 1, except that a floating plate replaces the floating gate as the floating charge-storage region. As will be explained in more detail below, the floating plate has silicon nano crystals that enhance field emissions and is at least an order of magnitude thinner (<10 nm) than the thickness of the floating gate.

The paragraph beginning at page 21, line 3 is amended as follows:

Figures 9 - 13 show relevant properties of silicon rich insulators (SRI) from the standpoint of charge trapping and charge injection or emission. Figure 9 is a graph showing refractive index of silicon-rich silicon nitride films versus SiH_2Cl_2/NH_3 flow rate ratio (R). This graph is provided herein to illustrate the known relationship between the silicon amount and the refractive index. The graph indicates that the index of refraction increases linearly with increasing silicon content. As such, the index of refraction of the films can be used as an indication of the silicon content of the films. The arrows on the graph illustrate experimental ratios.

The paragraph beginning at page 22, line 23 is amended as follows:

Silicon-rich nitride films having an R greater than 10 (or, more specifically, having an index of refraction greater than 2.3) are referred to as an injector medium. Silicon nitride injectors are preferred over silicon oxide injectors because of the superior high temperature stability of the former material. Silicon readily diffuses within silicon oxide at elevated processing temperatures, which disrupts the injection threshold by reducing the localized field distortions. However, even at higher processing temperature, silicon does not readily diffuse within Si_3N_4. A silicon-rich Si_3N_4 (SRN) injector provides appreciably enhanced charge conductance without providing appreciably enhanced charge trapping over stoichiometric Si_3N_4. This is illustrated in Figures [[3 and 4]] 11 and 12, which shows progressively reduced flatband

shifts for R=10 and R=15 with progressively increased conduction. The family of materials acting as injector material is identified as "i-SRN."

The paragraph beginning at page 24, line 25 is amended as follows:

Common dimensions for a typical NV FET device in the 0.13 to 0.15 μm technology generations are provided below. The cell size for a NAND gate is approximately 0.15 μm^2. The FET channel is approximately 150 nm wide. Both the floating gate and the PE are approximately 150 nm wide and about 250 nm thick. The tunnel oxide separating the floating gate from the FET channel [[is]] has a thickness 1529 of approximately 8 nm ~~thick~~. The ONO interpoly dielectric separating the PE and the floating gate is approximately 15 nm thick. The programming voltage applied to the PE is about 16 volts, and the pulse width of a programming pulse is approximately 1 ms. The field generated across the tunnel oxide is approximately 12 x 10^6 V/cm. The minimum program window (V_T("1") - V_T("0")) is approximately 2 V. The minimum program window is defined as the difference in the threshold voltages for a device with a stored one and a device with a stored zero. The endurance for a typical NV FET device is about 10^5 write/erase cycles. The power supply V_{DD} is 3.3 V.

The paragraph beginning at page 25, line 17 is amended as follows:

Figure 16 illustrates the capacitive coupling for a nonvolatile floating plate device. The device 1640 includes a control gate 1630 separated from a substrate 1612 by a gate insulator stack 1642 having a thickness 1629 of approximately 15 nm. The gate insulator stack 1642 includes a tunnel insulator 1644, charge centers 1646 that form a floating plate capable of storing charge, and a charge blocking dielectric 1648. A programming voltage VP_2 of 9.6 V is applied to the control gate 1630. As there is no separate floating gate, the coupling efficiency is 100%. The average electric field E_{AVG} between the control gate 1630 and the substrate 1612 is between about 6 to 7 x 10^6 V/cm.